Universe II™ Manual Addendum

December 23, 1999

Visit our Website at http://www.tundra.com
603 March Rd., Kanata, Ontario, K2K 2M5
Tel: (613) 592-0714 • 1-800-267-7231 • Fax: (613) 592-1320
support@tundra.com
Document Number : 8091142.AD001.04

The information in this document is subject to change without notice and should not be construed as a commitment by Tundra Semiconductor Corporation. While reasonable precautions have been taken, Tundra Semiconductor Corporation assumes no responsibility for any errors that may appear in this document.

Tundra® products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Tundra product could create a situation where personal injury or death may occur. Should Buyer purchase or use Tundra products for any such unintended or unauthorized application, Buyer shall indemnify and hold Tundra and its officers, employees, subsidiaries, affiliates and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Tundra was negligent regarding the design or manufacture of the part.

The acceptance of this document will be construed as an acceptance of the foregoing conditions.

Universe II™ Manual Addendum

This document complements revision 8091142.MD300.01 of the Universe II User Manual.

Document: 8091142.AD001.04

Printed in Canada

Table of Contents

For the latest Universe II and Universe IIB documentation please visit our web site — **http://www.tundra.com.**

1 Introduction

This document is a companion document to the Universe II User Manual — 8091142.MD300.01. This addendum explains the difference between the Universe II and Universe IIB, as well as highlighting design information for the Universe IIB. The addendum also corrects specific manual errata from the Universe II User Manual — 8091142.MD300.01.

This addendum is organized as follows:

- Section 2, “Universe II Device Errata” on page 1, informs the user that all Universe II Device Errata have been corrected in the Universe IIB device.
- Section 3, “Universe IIB Feature and Functional Changes” on page 2, describes feature and functional changes which have been incorporated in the Universe IIB.
- Section 4, “Universe IIB Design Information” on page 5, describes the Universe IIB design notes.
- Section 5, “Signals and DC Characteristics of the Universe IIB” on page 11, describes the signal and DC characteristics of the Universe IIB device.
- Section 6,“Mechanical Information” on page 19, describes package information for the Universe IIB device.
- Section 7, “Universe IIB Ordering Information” on page 23, outlines ordering information for the Universe IIB device.
- Section 8, “Universe II Manual Errata” on page 23, describes errata from the Universe II manual.

For more information on Universe II, please refer to the current Universe II User Manual — 8091142.MD300.01. For both Universe II and Universe IIB technical documentation refer to our web site — **http://www.tundra.com.**

2 Universe II Device Errata

All Universe II (CA91C142) device errata have been corrected in the Universe IIB (CA91C142B). Universe II errata are explained in the “Universe II (CA91C142) Device Errata” document, document number 8091142.ER600.08.

Refer to Tundra Semiconductor’s website — www. tundra.com — for the most up-to-date information on our VME product line.

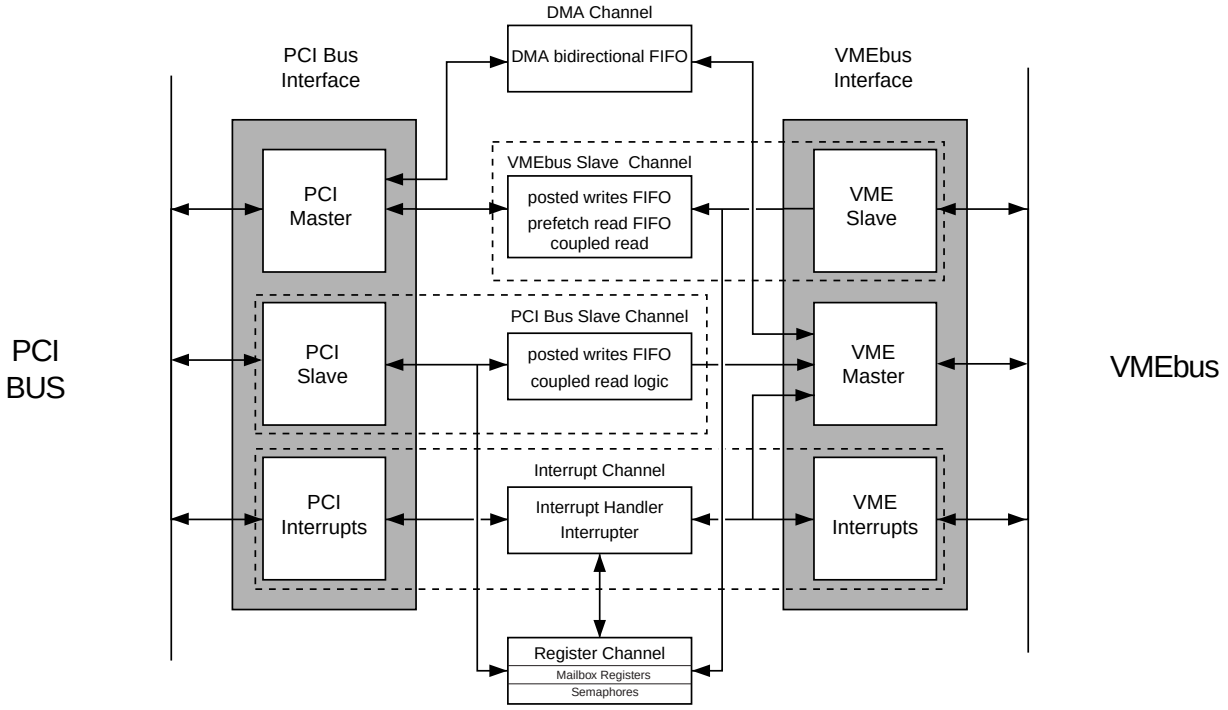
3 Universe IIB Feature and Functional Changes

This section identifies new features and changes in functionality implemented for the Universe IIB. The Universe IIB functionality and pin compatible with the Universe II.

3.1 Feature and Functional Changes

3.1.1 Universe IIB Block Diagram

Figure 1 Universe IIB Block Diagram



3.1.2 Universe IIB's FIFOs

Each of the Universe IIB's three FIFOs are double the depth of the Universe II FIFOs. The depth of FIFOs in the Universe II is 32 entries. The depth for the Universe IIB is 64 entries. The width of the FIFOs is 64-bit.

3.1.3 Revision ID

The revision ID of the Universe IIB is x02 in the PCI_CLASS register (offset x008).

3.1.4 VMEbus Arbiter Time-out Increased

The Universe IIB VMEbus arbiter time-out has been increased.

When the Universe II, acting as SYSCON, detected a false request — usually consisting of noise on the signal — on BR*, the device negated BGOUT* for 60 ns.

When false requests were performed with multiple masters, the 60 ns delay was insufficient. This delay was increased for the Universe IIB to ensure more reliable operation in the event of a false request on BR*.

3.1.5 DY4 Auto-ID

The Universe IIB initiates DY4 Auto-ID with IRQ1* when it is the SYSCON. In order for the SYSCON to be able to initiate a DY4 Auto-ID, it must be able to generate a level one interrupt and have its interrupt handler attempt to respond to it, but not detect a DTACK*.

3.1.6 DY4 Auto-ID

When using the DY4 Auto-ID mechanism in the Universe II, the propagation delay through the part from IACKIN* to IACKOUT* is five clocks instead of four. This causes existing DY4 Auto-ID algorithms to incorrectly identify relative Universe II boards in a system.

This issue has been changed to ensure Universe IIB boards are correctly identified in a system.

3.1.7 Noise on AS*, DS1* and DS0*

In the Universe II, noise on the AS*, DS1* and DS0* control signals may produce unpredictable operations, such as data corruption or false address qualification. Filters must be implemented in the designs.

In the Universe IIB, additional filters have been added in order to eliminate the noise on AS*, DS1* and DS0*. These filters can be activated by writing to bits 13 and 14 of the U2SPEC register at offset x4FC. For example, if a 1 is written to bit 13 the AS* filtering is activated. If a 1 is written to bit 14 then the DS0* and DS1* filters are activated.

Refer to Table on page 6 for information on the U2SPEC register.

3.1.8 DTACK* and AS* release

When performing IACK cycles and coupled 8- or 16-bit cycles as a VME master, the Universe II waited for the VME slave to release DTACK* before it removes AS*. If the slave card links release of DTACK* to the release of AS*, a deadlock condition may result because both master and slave wait for each other to end the cycle. The *ANSI VME64 Specification* specifies no slave relationship between DTACK* and AS*, therefore no assumptions on its behavior should be made by the slave.

The Universe IIB does not wait for DTACK* to be negated before negating AS*.

3.1.9 Increased delay

The delay between IRQ2* assertion and SYSFAIL* negation is increased in the Universe IIB. The Universe II negated SYSFAIL* as it asserted IRQ2* for VME64 Auto-ID.

To ensure correct operation of VME64 Auto-ID, the Universe IIB waits a few clocks cycles after asserting IRQ2* before negating SYSFAIL*.

3.1.10 Location Monitor

The location monitor can be accessed with an ADOH cycle with the Universe II. The location monitor cannot be accessed with an ADOH cycle with the Universe IIB.

3.1.11 Location Monitor

The Universe IIB VAS bit field in the LM_CTL register can be programmed to accept USER1 and USER2 AM codes.

3.1.12 VCSR_CTL

Bit 1 of the VCSR_CTL register is reserved in the Universe IIB.

3.1.13 SYSRESET*

A software SYSRESET* bit has been added in the Universe IIB. When bit 14 of the MISC_CTL register is written with a value of 1, the Universe IIB asserts SYSRESET*. However, the Universe IIB ignores all input on SYSRESET* while it asserts SYSRESET*. This permits the Universe IIB to assert SYSRESET* without resetting itself.

3.1.14 PCI Target

Transfers appear on the VMEbus as 16-bit transfers when the Universe IIB is programmed as follows:

- PWEN= 1
- VDW=16-bit, 32-bit or 64-bit
- VCT= 0
- External PCI master begins a burst 32-bit write with A2=0 and BE#=0011, followed by a transfer with BE#=1100.

These criteria optimize performance of 32-bit PCI systems which regularly perform 16-bit transfers. A series of 16-bit transfers is also performed if 64-bit posted write is received with BE#=11000011.

3.1.15 Latency Timer

When the Universe IIB latency timer is programmed for eight clock periods and FRAME#, IRDY# and TRDY# are asserted while GNT# is not asserted, FRAME# is negated on the next clock edge.

3.1.16 Interrupt Acknowledge Priority

The interrupt handler in the Universe II serviced the interrupt depending on the order the interrupt was received. When an interrupt of higher priority was received, the Universe II serviced the interrupt it received first, even if it has a lower priority designation. The Universe IIB services an interrupt of higher priority first instead of the first interrupt it receives.

4 Universe IIB Design Information

4.1 Universe IIB Specific Register

The Universe Specific Register, U2SPEC, offset 0x4FC, can be used to improve the performance of the Universe IIB by reducing the latency of key VMEbus timing elements. This register is present in versions of the Universe device which have a Revision ID of 01or 02 — defined in the PCI_CLASS register, offset 008.

This feature exists in the Universe II, and is described in detail in document 8091C142.MD001.01. Please refer to the Tundra website — www.tundra.com — for more information.

This section describes the operation of the Universe IIB's Specific register (U2SPEC), offset 0x4FC.

4.1.1 Overview of the U2SPEC Register

Although the VMEbus is asynchronous, there are a number of maximum and minimum timing parameters which must be followed. These requirements are detailed in the *VME64 Specification*.

In order to qualify as compliant the master, slave and location monitor devices must guarantee they meet these timing parameters independent of their surroundings. They must assume zero latency between themselves and the VMEbus. This, in practice, is never the case. Buffers, transceivers and the backplane itself, all introduce latencies that combine to produce additional system delay. The consequence of such delay is the degradation of overall performance.

The Universe IIB's U2SPEC register enables users to compensate for the latencies which are inherent to their VMEbus system designs. Through the use of this register, users can reduce the inherent delay associated with five key VMEbus timing parameters.

Use of the U2SPEC register may result in violation of the VME64 Specification.

The key VMEbus timing parameters are outlined in the following sections. The Universe II and Universe IIB's U2SPEC register bits are described in Table .

Table 1 Universe II and IIB Specific Register (U2SPEC)

Register Name: U2SPEC	Offset: 4FC

Bits	Function							
31-24	Universe Reserved							
23-16	Universe Reserved							
15-08	Universe Reserved	DS0/DS1	AS	DTKFLTR	Reserved	MASt11	READt27	
07-00	Universe Reserved					POSt28	Reserved	PREt28

U2SPEC Description

Name	Type	Reset By	Reset State	Function
DS0/DS1	R/W	all	0	Data Strobe Filtering 0=Disable, 1=Enable
AS	R/W	all	0	Address Strobe Filtering 0=Disable, 1=Enable
DTKFLTR	R/W	all	0	VME DTACK* Inactive Filter 0=Slower but better filter, 1=Faster but poorer filter
MASt11	R/W	all	0	VME Master Parameter t11 Control (DS* high time during BLT's and MBLT's) 0=Default, 1=Faster
READt27	R/W	all	00	VME Master Parameter t27 Control (Delay of DS* negation after read) 00=Default, 01=Faster, 10=No Delay
POSt28	R/W	all	0	VME Slave Parameter t28 Control (Time of DS* to DTACK* for posted-write) 0=Default, 1=Faster
PREt28	R/W	all	0	VME Slave Parameter t28 Control (Time of DS* to DTACK* for prefetch read) 0=Default, 1=Faster

The bits marked as Universe Reserved must be set to "0".

4.1.2 Adjustable VME Timing Parameters

4.1.2.1 VME DTACK* Inactive Filter (DTKFLTR)

In order to overcome the DTACK* noise typical of most VME systems, the Universe IIB quadruple samples this signal with the 64 MHz clock. The extra sampling is a precaution that results in decreased performance. Users who believe their systems to have little noise on their DTACK* lines can elect to filter this signal less, and thus increase their Universe II and Universe IIB response time.

4.1.2.2 VME Master Parameter t11 Control (MASt11)

According to the *VME64 Specification*, a VMEbus master must not drive DS0* low until both it and DS1* have been simultaneously high for a minimum of 40 ns. The MASt11 parameter in the U2SPEC register, however, allows DS0* to be driven low in less than 40 ns.

4.1.2.3 VME Master Parameter t27 Control (READt27)

During read cycles, the VMEbus master must guarantee the data lines are valid within 25 ns after DTACK* is asserted. The master must not latch the data and terminate the cycle for a minimum of 25 ns after the falling edge of DTACK*.

The READt27 parameter in the U2SPEC register supports faster cycle termination with one of two settings. One setting allows data to be latched and the cycle terminated with an associated delay that is less than 25 ns. The second setting results in no delay in latching and termination.

4.1.2.4 VME Slave Parameter t28 Control (POSt28)

According to the *VME64 Specification*, VMEbus slaves must wait at least 30 ns after the assertion of DS* before driving DTACK* low. When the Universe II or Universe IIB is acting as a VME slave, the POSt28 parameter in the U2SPEC register enables DTACK* to be asserted in less than 30 ns when executing posted writes.

4.1.2.5 VME Slave Parameter t28 Control (PREt28)

VMEbus slaves must wait at least 30ns after the assertion of DS* before driving DTACK* low. When the Universe II or Universe IIB is acting as a VME slave in the transaction, PREt28 parameter in the U2SPEC register enables DTACK* to be asserted in less than 30 ns when executing pre-fetched reads.

4.2 Universe IIB Non-incrementing DMA

This section describes the operation of the Universe IIB's VMEbus Non-Incrementing Mode (Non-Inc Mode) for DMA transfers. The Non-Inc Mode only applies to versions of the Universe device that have a Revision ID of 01 and 02 - defined in the PCI_CLASS register, offset 008.

This feature exists in the Universe II, and is described in detail in document 8091C142.MD003.01. Please refer to the Tundra website, www.tundra.com, for more information.

4.2.1 Feature Overview

The Non-Inc Mode allows the DMA Controller to perform transfers to or from a fixed VMEbus address. This means that the specified VMEbus address is not incremented during DMA reads or writes. This applies to both Direct and Linked List types of DMA operation. For more information on these two types of DMA operation, refer to the DMA Controller Section in the Universe II User Manual.

Unlike incrementing DMA operation, in Non-Inc Mode the DMA Controller can only perform 8-,16- or 32-bit single cycle transfers on the VMEbus. This means that BLT and MBLT transfers cannot be performed when operating in Non-Inc Mode.

4.2.2 How to Use Non-Inc Mode

The VMEbus Non-Inc Mode is enabled by writing a 1 to bit 9 of the DCTL register, offset 0x200. This bit is called the NO_VINC bit and is shown as Universe Reserved in Universe and Universe II documentation.

Table 2 DMA Transfer Control Register (DCTL)

Register Name: DCTL	**Offset:200**

Bits	Function					
31-24	L2V	Universe Reserved				
23-16	VDW		Universe Reserved		VAS	
15-08	PGM		SUPER	Universe Reserved	NO_VINC	VCT
07-00	LD64EN	Universe Reserved				

In order to set-up and initiate DMA operation, the same steps which are described in the DMA Controller Section in the Universe II User Manual must be followed for Non-Inc Mode.

The basic steps in setting-up and initiating DMA operation are as follows:

1. Program the tenure and interrupt requirements in the DGCS register (offset 0x220).
2. Program the source and destination addresses in the DLA and DVA registers.
3. Set the GO bit in the DGCS register.

4.2.3 Issues with Non-Inc Mode

4.2.3.1 The VMEbus Address

In Non-Inc Mode, the DVA register (offset 0x210) does not necessarily contain the fixed VMEbus address. This register must not be read during a DMA Non-Inc Mode transfer. Once a DMA transfer has been stopped — by setting the STOP bit of the DGCS register — the Non-Inc Mode transfer cannot be restarted by simply writing a “1” to the GO bit of the DGCS register. The DVA register must be reprogrammed with the required address before setting the DGCS GO bit.

4.2.3.2 The VON Counter

When the VON counter in the DGCS register reaches its programmed limit, the VMEbus Master Interface of the Universe II stops transferring data until the VOFF timer expires. If the device is operating in Non-Inc Mode, the VON counter has different limits than those indicated in the DMA Controller section in the Universe II User Manual.

The different settings are detailed in Table 3.

Table 3 VON Settings for Non-Inc Mode

VON	VMEbus Aligned DMA Transfer Count
001	128 bytes
010	256 bytes
011	512 bytes
100	1024 bytes
101	2048 bytes
110	4096 bytes
111	8192 bytes

4.2.3.3 P_ERR Flag Behavior

When the GO bit is set in Non-Inc Mode, the P_ERR flag of the DGCS register is 1 when the following conditions are true:

- VCT bit of the DCTL register has a value of 1
- VDW field of the DCTL register has a value of 01 and bit 0 of the DVA register is a value of 0
- VDW field of the DCTL register has a value of 10 and bits 1 and 0 of the DVA register are non-zero

- VDW field of the DCTL register has a value of 11.

4.2.3.4 Single Cycle Transfers

The Universe II and Universe IIB perform 8-,16- or 32-bit single cycle transfers on the VMEbus. BLT and MBLT transfers cannot be performed when operating in Non-Inc Mode.

4.2.4 Performance

The transfer performance of DMA in Non-Inc Mode has been simulated at 14 MB/s for 32-bit writes and at 8 MB/s for 32-bit reads. This performance was determined using ideal slave responses; lower performance can be expected in actual systems.

5 Signals and DC Characteristics of the Universe IIB

5.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Rating

Parameter	Limits
DC Supply Voltage	-0.3 to 7.0 V
DC Input Voltage	-0.5 to vdd + 0.5V
DC current drain per pin, any single input or output	± 50ma
DC current drain per pin, any paralleled outputs	± 100ma
DC current drain Vdd or Vss	± 75ma
Storage Temperature (Tstg)	-40 ºC to 125 ºC

5.2 Recommended Operating Characteristics

The following table specifies recommended operating condition for the Universe IIB.

Table 5 Operating Conditions

Symbols	Parameters	Min	Max	Frequency Operation (Mhz)
Vdd	DC Supply Voltage (5V ± 10%)	4.5V	5.5V	
Ta (Commercial)	Ambient Temperature	0ºC	+70ºC	25 - 33
Ta (Industrial)	Ambient Temperature	-40ºC	+85ºC	25 - 33
Ta (Extended)	Ambient Temperature	-55ºC	+125ºC	25

5.2.1 Non-PCI Characteristics

The following table specifies the required DC characteristics of all non PCI signals pins:

Table 6 Non-PCI Electrical Characteristics

Symbols	Parameters	Test conditions	Min	Max
VIH_ttl	Voltage Input high		2.0 V	
VIH_cmos	Voltage Input high		0.7 Vdd	
VIL_ttl	Voltage Input low			0.8V
VIL_cmos	Voltage Input low			0.3Vdd

Table 6 Non-PCI Electrical Characteristics

Symbols	Parameters	Test conditions	Min	Max
Vt+_ttl	Voltage Input high Schmitt trigger		2.0 V	
Vt+_cmos	Voltage Input high Schmitt trigger		0.7Vdd	
Vt-_ttl	Voltage Input low Schmitt trigger			0.8V
Vt-_cmos	Voltage Input low Schmitt trigger			0.25Vdd
Iin	Input leakage current low	With no pull-up or pull-down resistance (Vin = Vss or Vdd)	-5.0µa	5.0µa
Ioz	Tristate output leakage	Vout = vdd or Vss	-10.0µa	10.0µa

5.2.2 PCI Characteristics

The following table specify the required AC and DC characteristics of all PCI Universe IIB signal pins. Reference document is the PCI Local Bus specification Revision 2.1 and the Aspec Document describing 5.0 V PCI (75 µm pitch) in the HDA/C9000 process.

Table 7 AC/DC PCI Electrical Characteristics

Symbols	Parameters	Condition	Min	Max	Units
Vil	Voltage Input low		-0.5	0.8	V
Vih	Voltage Input high		2.0	Vdd + 0.5	V
Iih	Input leakage current high	Vin = 2.7V		70	µa
Iil	Input leakage current low	Vin = 0.5V		-70	µa
Vol	Voltage output low	Iout = 3ma, 6ma		0.4	V
Voh	Voltage output high	Iout = 2ma	2.4		V
Ioh(AC)	Switching current high	0 < Vout[2]1.4	-44		ma
		1.4 < Vout < 2.4	-44 + (Vout -1.4) / 0.024		ma
		3.1 < Vout < Vdd		EqnA	ma
	(Test point)	Vout = 3.1V		-142	ma
Iol (AC)	Switching current high	0 < Vout[3]1.4	95		ma
		0.6Vdd < Vout < 0.1Vdd	Vout / 0.023		ma

Table 7 AC/DC PCI Electrical Characteristics

Symbols	Parameters	Condition	Min	Max	Units
		0.71 < Vout < 0		EqnB	ma
	(Test point)	Vout = 0.71V		206	ma
Icl	Low clamp current	-5 Vin^2-1	-25 + (Vin +10) / 0.015		ma
slewr	Output rise slew rate	0.4V to 2.4V load	1	5	V/ns
slewf	Output fall slew rate	2.4V to 0.4V load	1	5	V/ns

Eqn A : Ioh = 11.9 * (Vout - 5.25) * (Vout + 2.45) for Vdd > Vout > 3.1V
Eqn B : Iol = 78.5 * Vout * (4.4 - Vout) for 0V < Vout < 0.71V

5.2.3 313 PBGA Pin List

Refer to the Universe II User Manual for information on the 313 PBGA pin list.

5.2.4 361 DBGA Pin List

Table 8 DBGA Pin List

DBGA_361	Pin	DBGA_361	Pin	DBGA_361	Pin
E05	vd<20>	K02	vrbbsy_	P06	int_<3>
E04	vd<19>	J04	int_<7>	P04	ad<25>
E06	vd<18>	H06	int_<6>	V03	ad<57>
G08	vd<17>	J01	vscon_dir	N06	ad<24>
E03	vd<16>	K07	vxsysfail	T02	vrbr_<0>
D02	vd<15>	K04	vsysclk	P05	ad<56>
F04	vd<14>	J05	vbclr_	T03	int_<1>
D03	vd<13>	K06	ad<31>	N04	ad<23>
F02	vd<12>	K03	ad<63>	R02	pll_testsel
F05	vd<11>	K05	vxbbsy	W04	lclk
G02	vd<10>	L02	par	V02	pll_testout
D01	vd<9>	L01	lrst_	T04	AVSS
G05	vd<8>	L06	ad<30>		
E02	vd<7>	M07	ad<62>		
G03	vd<6>	L03	vrbr_<2>		
G06	vd<5>	N01	vrbr_<1>		
G09	vd<4>	L04	ad<29>		
G01	vd<3>	M02	ad<61>		
H05	vd<2>	L05	ad<28>		
E01	vd<1>	P02	pwrrst_		
H04	vd<0>	M04	ad<60>		
H02	vrbr_<3>	N02	ad<27>		
H07	int_<5>	M05	ad<59>		
J03	int_<4>	N03	ad<26>		
J02	int_<2>	R01	ad<58>		

Table 7 DBGA Pin List (continued)

DBGA_361	Pin	DBGA_361	Pin	DBGA_361	Pin
T06	AVDD	R08	ad<16>	P12	req64_
R04	vcoctl	N07	ad<48>	T14	ad<13>
N10	serr_	Y08	cbe<7>	Y15	enid
Y05	perr_	V11	cbe<6>	T15	ad<45>
V05	ad<55>	W09	cbe<3>	V14	stop_
T05	ad<22>	P08	vrsysfail_	W17	ad<12>
V07	devsel_	R09	cbe<2>	R12	ad<44>
R06	ad<54>	W11	tmode<0>	W16	rst_
W07	ad<21>	T12	cbe<5>	V15	ad<11>
W05	par64	Y09	cbe<1>	V17	tmode<1>
T08	ad<53>	Y11	cbe<4>	R13	ad<43>
V06	trdy_	P09	cbe<0>	W15	viacki_
P07	ad<20>	N16	ad<15>	V18	ad<10>
N13	ad<52>	V13	irdy_		
T09	ad<19>	Y12	gnt_		
Y04	ad<51>	R11	vrirq_<5>		
V09	ad<18>	W12	ad<47>		
Y07	ack64_	P11	frame_		
N14	ad<50>	Y13	idsel		
R07	ad<17>	T11	ad<14>		
W08	ad<49>	W13	ad<46>		

Table 7 DBGA Pin List (continued)

DBGA_361	Pin	DBGA_361	Pin	DBGA_361	Pin
Y16	ad<42>	K14	vxirq<7>	H15	vxbr<1>
R14	ad<9>	L15	vracfail_	G10	int_<0>
R16	lock_	L19	vxbr<2>	G12	vrirq_<4>
N17	ad<41>	K15	ad<0>	F18	vrirq_<3>
P13	ad<8>	K18	ad<33>	F16	vrirq_<2>
T16	ad<40>	L14	vbgi_<3>	G18	vrirq_<1>
P14	ad<7>	J13	vbgi_<2>	C16	vxbr<3>
P15	tmode<2>	J15	vbgi_<1>	G11	va<31>
R18	vme_reset_	K16	vbgi_<0>	E19	va<30>
P16	ad<39>	K13	vbgo_<3>	G17	va<29>
T17	ad<6>	K17	vbgo_<2>	E18	va<28>
N19	ad<38>	J19	vbgo_<1>	F15	va<27>
R19	ad<5>	J14	vbgo_<0>	E17	va<26>
N18	ad<37>	H13	ad<32>	B17	va<25>
M15	ad<4>	J18	vxirq<6>		
P18	ad<36>	J17	vxirq<5>		
T18	ad<3>	G15	vxirq<4>		
M16	ad<35>	J16	vxirq<3>		
M18	ad<2>	H18	vxirq<2>		
M13	ad<34>	H14	vxirq<1>		
L16	ad<1>	G19	req_		
L17	vrirq_<7>	H16	viacko_		
L18	vrirq_<6>	G14	vxbr<0>		

Table 7 DBGA Pin List (continued)

DBGA_361	Pin	DBGA_361	Pin	DBGA_361	Pin
C17	va<24>	F11	vslave_dir	E10	vam<2>
D12	clk64	D14	va<5>	A07	vam<1>
C13	vrsysrst_	D11	va<4>	D06	vam<0>
E16	vxsysrst	B11	va<3>	B06	vrberr_
F13	va<23>	D13	va<2>	E09	vam_dir
E15	va<22>	E13	va<1>	F07	vd_dir
C15	va<21>	A12	vas_	C07	vd<31>
D18	va<20>	D09	vlword_	A05	vd<30>
D19	va<19>	B10	va_dir	D05	vd<29>
C12	va<18>	E12	tdo	B05	vwrite_
B15	va<17>	F09	tdi	C02	vd<28>
B14	va<16>	D08	vas_dir	E08	vd<27>
B16	va<15>	B09	trst_	B03	vd<26>
D17	va<14>	C09	voe_	C05	vd<25>
A15	va<13>	A11	tck	C04	vd<24>
B13	va<12>	A09	vds_<1>	E07	viack_
E14	va<11>	E11	vds_<0>	B04	vd<23>
F12	va<10>	F08	vds_dir	C03	vd<22>
A13	va<9>	B08	vxberr	A04	vd<21>
D15	va<8>	C08	tms		
A16	va<7>	A08	vam<5>		
C11	va<6>	D07	vam<4>		
B12	vdtack_	B07	vam<3>		

Table 8 Ground[a], Power and N/C[b]

DBGA_361	Pin	DBGA_361	Pin	DBGA_361	Pin	DBGA_361	Pin	DBGA_361	Pin
A03	Vdd	M03	Vdd	A14	Vss	K12	Vss	V08	Vss
A06	Vdd	M14	Vdd	A17	Vss	L07	Vss	V19	Vss
A10	Vdd	M19	Vdd	B02	Vss	L08	Vss	W02	Vss
C01	Vdd	N05	Vdd	B18	Vss	L09	Vss	W10	Vss
C06	Vdd	N09	Vdd	C18	Vss	L10	Vss	W18	Vss
C10	Vdd	P03	Vdd	F06	Vss	L11	Vss	Y03	Vss
C14	Vdd	P17	Vdd	F10	Vss	L12	Vss	Y06	Vss
C19	Vdd	R03	Vdd	G04	Vss	L13	Vss	Y14	Vss
D04	Vdd	R05	Vdd	G16	Vss	M06	Vss		
D10	Vdd	R10	Vdd	H08	Vss	M08	Vss		
D16	Vdd	R15	Vdd	H09	Vss	M09	Vss		
F01	Vdd	T01	Vdd	H10	Vss	M10	Vss		
F03	Vdd	T07	Vdd	H11	Vss	M11	Vss		
F14	Vdd	T13	Vdd	H12	Vss	M12	Vss	A01	nc
F17	Vdd	T19	Vdd	J06	Vss	M17	Vss	A02	nc
F19	Vdd	V04	Vdd	J07	Vss	N08	Vss	A18	nc
G07	Vdd	V10	Vdd	J08	Vss	N11	Vss	A19	nc
G13	Vdd	V12	Vdd	J09	Vss	N12	Vss	B01	nc
H01	Vdd	V16	Vdd	J10	Vss	N15	Vss	B19	nc
H03	Vdd	W03	Vdd	J11	Vss	P01	Vss	W01	nc
H17	Vdd	W06	Vdd	J12	Vss	P10	Vss	W19	nc
H19	Vdd	W14	Vdd	K08	Vss	P19	Vss	Y01	nc
K01	Vdd	Y10	Vdd	K09	Vss	R17	Vss	Y02	nc
K19	Vdd	Y17	Vdd	K10	Vss	T10	Vss	Y18	nc
M01	Vdd			K11	Vss	V01	Vss	Y19	nc

a. *Vdd/VSS pad placements have been based on SSN and Outside location considerations.*

b. Route all nc signals out to vias on your board to allow for future migration to Universe variants

Route all nc signals out to vias on your board to allow for future migration to Universe variants

6 Mechanical Information

6.1 Universe IIB 313 PBGA

Please refer to the Mechanical and Ordering Information in the Universe II User Manual for information on the 313 PBGA package.

The 313 Universe IIB (CA91C142B) PBGA has a four layer substrate design. The previous version of the 313 PBGA had a two layer substrate design. Please refer to *Application Note: 313 PBGA Package Differences for the Universe II and Universe IIB*, document number 8091142.AN004.01, for more information on the package differences.This document is available on the Tundra website — ww.tundra.com.

6.2 Universe IIB 361 DBGA Packaging

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5-1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. SOLDER BALL POSITION DESIGNATION PER JEDEC PUBLICATION 95-1. STANDARD PROCEDURES AND PRACTICES SPP-010.
4. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
5. THIS DRAWING COMPLIES WITH JEDEC REGISTERED OUTLINE MO-156, VARIATION BBJ

6 THIS DIMENSION INCLUDES STANDOFF HEIGHT "A1", PACKAGE BODY THICKNESS AND LID HEIGHT.

7 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C- .

8 PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

SYMBOL	ALL DIMENSIONS IN MILLIMETERS			
	MIN.	NOM.	MAX.	NOTE
A	2.89	3.28	3.67	
A_1	0.58	0.64	0.70	
b	0.80	0.85	0.90	
A_2	1.14	1.27	1.40	
D	24.75	25.00	25.25	
D_1	22.63	22.86	23.09	
E	24.75	25.00	25.25	
E_1	22.63	22.86	23.09	
e	1.27 BSC			
aaa	0.15			
bbb	0.25			
ccc	0.35			
ddd	0.20			

Figure 2 DBGA Packaging (continued)

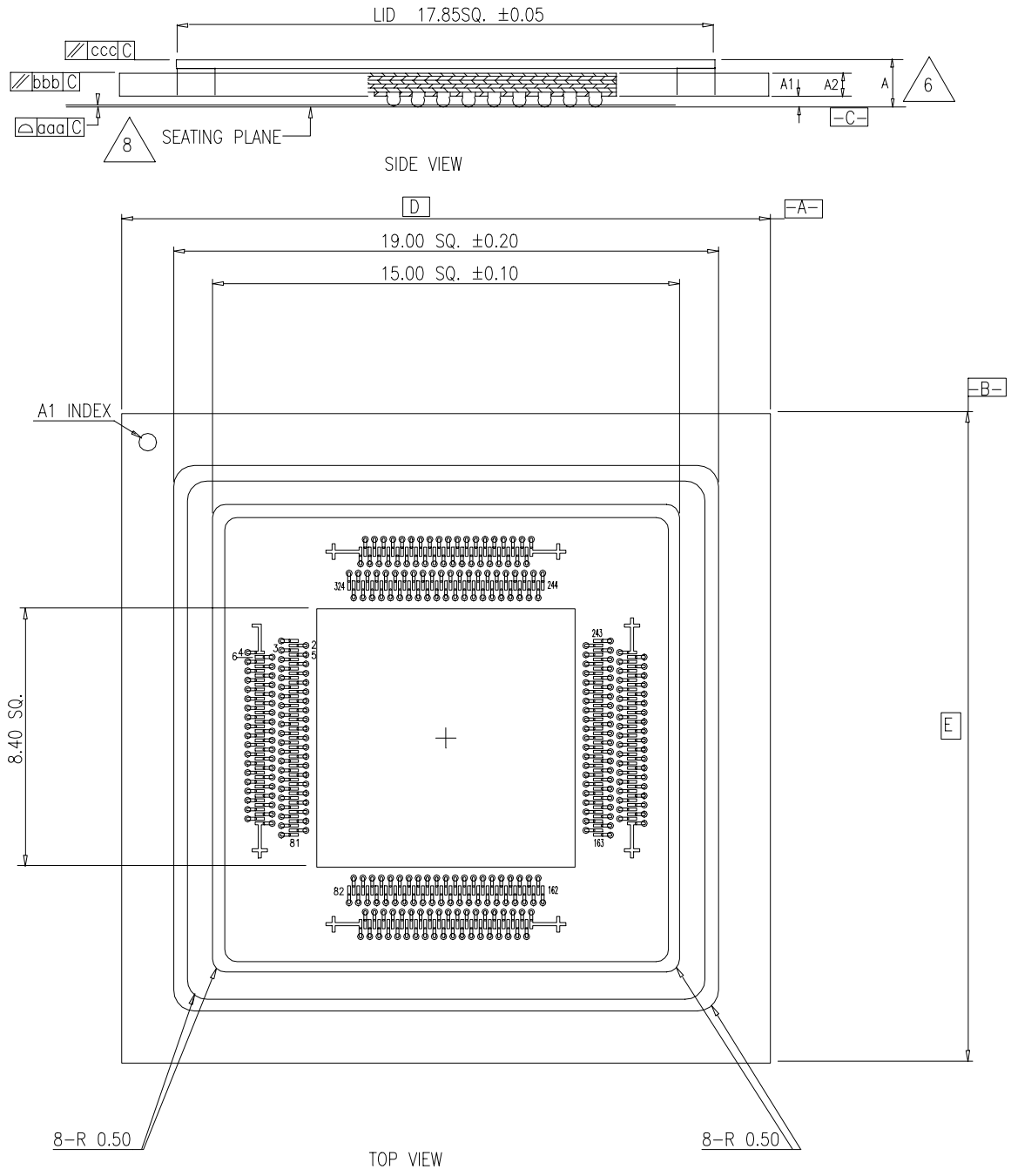
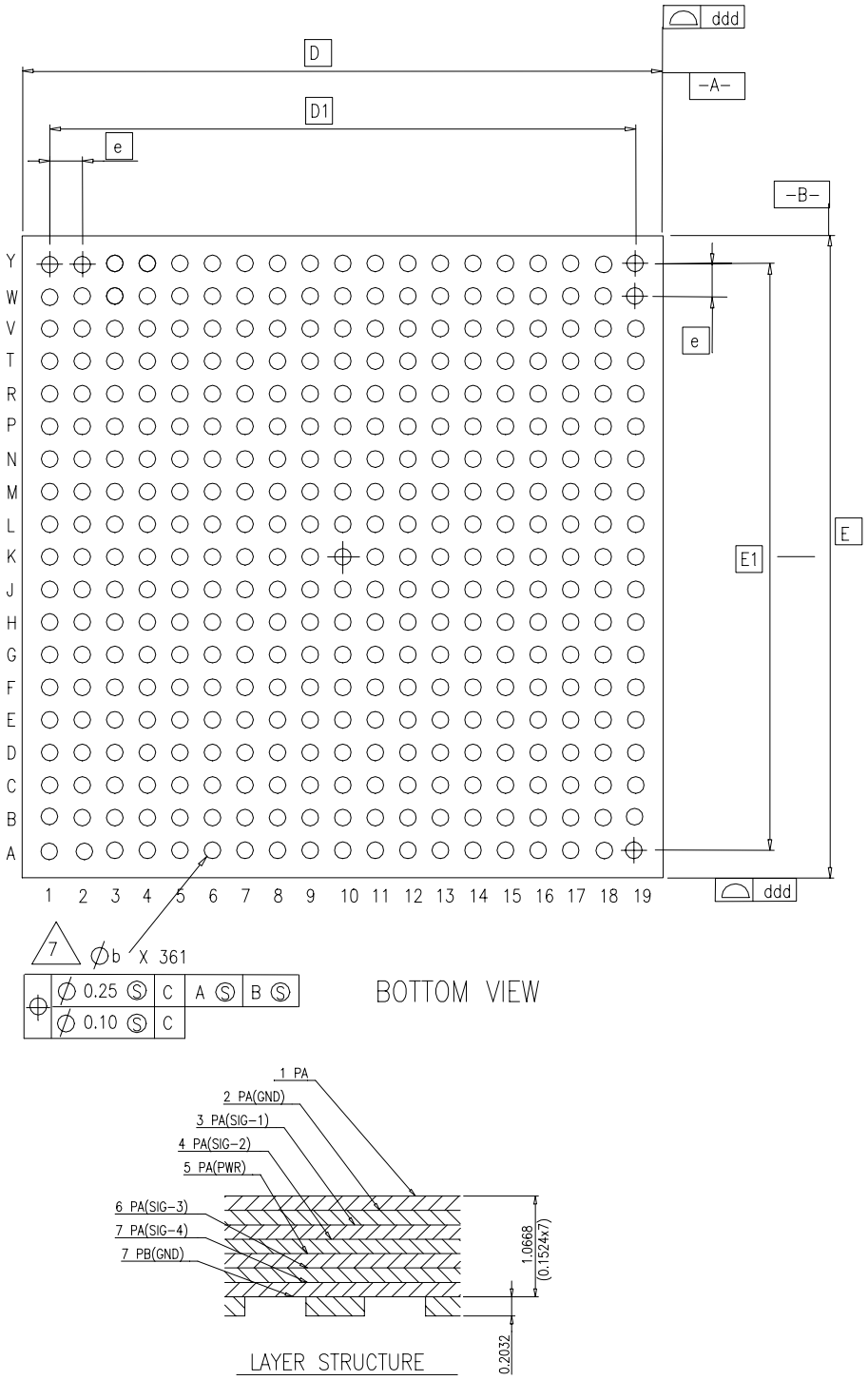


Figure 2 DBGA Packaging (continued)



7 Universe IIB Ordering Information

Table 9 Ordering Information[a]

Part Number	Frequency	Voltage	Temperature	Package
CA91C142B-33CE	33 MHz	5.0V	0° to 70°C	PBGA
CA91C142B-33IE	33 MHz	5.0V	-40° to 85° C	PBGA
CA91C142B-25EEZ	25 MHz	5.0V	-55° to 125°C	PBGA
CA91C142B-33CBZ	33 MHz	5.0V	0° to 70°C	DBGA
CA91C142B-33IBZ	33 MHz	5.0V	-40° to 85° C	DBGA
CA91C142B-25EBZ	25 MHz	5.0V	-55° to 125°C	DBGA

a. The extended temperature Universe IIB is only available in 25 MHz variants.

8 Universe II Manual Errata

8.1 Universe II Manual Errata

This section corrects manual errata in the Universe II User Manual — 8091142.MD300.01.

Chapter 1

Page No: 1-5

Errata Description: The fifth bulleted point, Phone Support, has the wrong phone number.

Corrective Action: The phone number for Phone Support is (613) 592-0714.

Chapter 2

Page No: 2-8 (Section 2.2.1.3)

Errata Description: The first bullet implies there is another option than the TXFE bit being clear when the TXFIFO is empty.

Corrective Action: Replace existing bulleted text with: “when the TXFIFO is empty the TXFE bit is clear”.

Page No: 2-18 (second paragraph)

Errata Description: The first sentence read 1024-byte boundary.

Corrective Action: The byte boundary should be 2048-byte.

Page No: 2-18 (last paragraph)

Errata Description: The first two sentences of this paragraph are incorrect.

Corrective Action: Replace existing text with: “If an error occurs on the PCI bus, a bus error will occur on the VMEbus because they are coupled. In the event a bus error occurs on the VMEbus once a LOCK# has been established, the VMEbus master which locked the VMEbus must terminate the LOCK# by negating BBSY*.”

Page No: 2-19 (first paragraph)

Errata Description: Clarification of information required.

Corrective Action: Add the following note to the paragraph: “LOCK# is negated on the PCI bus when AS* is negated on the VMEbus. LOCK# is not negated when AS* is negated if LOCK# was asserted by an ADOH/lock command.”

Page No: 2-24 (last paragraph)

Errata Description: The paragraph references a level 2 STATID register, which does not exist.

Corrective Action: Remove the word level 2 in reference to the STATID register.

Page No: 2-31 (Section 2.3.1.1)

Errata Description: The paragraph incorrectly references the PCI target response of ACK64#.

Corrective Action: Delete the last two sentences in this paragraph. The Universe II will pack write data to 64-bits for the first data phase if it asserted REQ64# independent of whether or not it receives ACK64# from the target.

Page No: 2-36 (Section 2.3.2.1)

Errata Description: The first bullet implies there is another option then the MISC_STAT register being clear when the RXFIFO is emptying.

Corrective Action: Replace existing bulleted text with: “when the RXFIFO is emptying the MISC_STAT register is clear”.

Page No: 2-38 (Section 2.3.3.1)

Errata Description: The text incorrectly explains when the Universe II becomes PCI bus target.

Corrective Action: Change the text of eight programmed PCI target images to nine programmed PCI target images.

Page No: 2-42 (Section 2.3.3.3)

Errata Description: The explanation of Coupled Request Phase is incorrect.

Corrective Action: Delete Coupled Request Phase information.

Page No: 2-51 (Section 2.4.1.1)

Errata Description: The VMEbus slave image 0 and 5 is incorrect.

Corrective Action: Replace existing text with: (VMEbus slave image 0 and 4).

Page No: 2-51 (Section 2.4.1.1)

Errata Description: The third paragraph on the page, concerning VMEbus slave images, is incorrect.

Corrective Action: Replace existing text with: The Universe II's eight VMEbus slave images (images 0 to 7) are bounded by A32 space. The first and fourth of these images (VMEbus slave image 0 and 4) have a 4-Kbyte resolution while VMEbus slave images 1 to 3 and 5 to 7 have 64-Kbyte resolution (maximum image size of 4 Gbytes). Image 0 or 4 would be used as A16 images since they provide the finest granularity of the eight images.

Page No: 2-51 (Section 2.4.1.2)

Errata Description: The field which controls generation of the PCI transaction command was named incorrectly.

Corrective Action: Replace PAS with LAS.

Page No: 2-116 (Table 2.22)

Errata Description: The last entry in the table, PCI CSR Image Space, has an incorrect title.

Corrective Action: Replace PCI CSR Image Space with PCI CSR Master Enable.

Page No: 2-123 (Section 2.10.5)

Errata Description: The minimum duty cycle value is incorrect.

Corrective Action: The text should be corrected from 60-40 duty cycle to 50-50 duty cycle.

Chapter 3

Page No: 3-3 (Table 3.1)

Errata Description: More information is required for the VOE# signal description.

Corrective Action: Add the sentence: VOE# is negated during some VMEbus Slave Channel read operations.

Page No: 3-6 (Table 3.2)

Errata Description: The SERR# signal is not bidirectional.

Corrective Action: The SERR# signal should be changed to an output.

Appendix A

Page No: App A-1

Errata Description: The last sentence describing bit combinations is incorrect.

Corrective Action: Replace existing text with: “Bits listed as reserved must be programmed with a value of zero. Reserved bits will always read a value of zero.”

Page No: App A-8

Errata Description: The DP_D functional description and the reset state must be corrected.

Corrective Action: The reset state of DP_D is 0. The function information of Data Parity Detected must be renamed Master Data Parity Error.

Page No: App A-36

Errata Description: The reset state for CRT[3:0] and the functional description for CWT[2:0] must be corrected.

Corrective Action: Change the reset state for CRT[3:0] to 0001. Change the 101=246 PCI Clocks to 256 PCI Clocks.

Page No: App A-40

Errata Description: The LAERR Description has an incorrect name.

Corrective Action: Alter LAERR [31:0] to LAERR [31:2].

Page No: App A-44

Errata Description: The PCI Target Image 4 Translation Offset (LS14_TO) has an incorrect offset value.

Corrective Action: Change Offset:1B0 to Offset:1AC.

Page No: App A-65

Errata Description: Throughout the LINT_EN Description, the Interrupt is referred to as masked and should, instead, be referred to as disabled.

Corrective Action: Correct the table to read disabled instead of masked.

Page No: App A-68

Errata Description: The LINT_STAT Description from VERR to VOWN describes the interrupts as enables when they should be called active since they are status bits.

Corrective Action: Correct the appropriate descriptions to refer to the Interrupts as active instead of enabled.

Page No: App A-92 (Table A.80)

Errata Description: The Semaphore 1 Register Table (SEMA1) should have a function of TAG7 for bits 31-24, SEM7.

Corrective Action: Replace the TAG6 function with TAG7.

Page No: App A-94 (fourth paragraph)

Errata Description: The PWON setting was misspelled POWN.

Corrective Action: Replace POWN with PWON.

Page No: App A-94 (sixth paragraph)

Errata Description: The last paragraph concerning the PABS[1:0] field contains incorrect data.

Corrective Action: Delete the entire paragraph.

Page No: App A-95

Errata Description: The MISC_CTL Description table, has incorrect values for SW_LRST and SW_SYSRST.

Corrective Action: The Type column for SW_LRST and SW_SYSRST should change to: W/Read 0 always.

Page No: App A-95 (Table A.82)

Errata Description: The SW_SYSRST bit is misspelled in the table.

Corrective Action: Replace SW_SRST with SW_SYSRST.

Page No: App A-97

Errata Description: The Function description for the LCLSIZE in the MISC_STAT Description table is incorrect.

Corrective Action: Replace the part of the sentence that states: At the trailing edge of RST#, with: At the rising edge of RST#.

Page No: App A-97

Errata Description: The MISC_STAT Description table has incorrect values for DY4AUTOID.

Corrective Action: Replace the Reset By column for DY4AUTOID with: Power-up Reset and VMEbus SYSRESET*.

Page No: App A-115

Errata Description: Information must be added to the VAS Function in the LM_CTL Description table.

Corrective Action: Add, to the VAS Function section of the LM_CTL Description table, the following information: 110=User1, 111=User2.

Page No: App A-116

Errata Description: The Name BS[31:16] is incorrect in the LM_BS Description.

Corrective Action: Replace the Name BS[31:16] with BS[31:12].

Page No: App A-119

Errata Description: Table A.105, VCSR_CTL, should show bit 1 as reserved.

Corrective Action: Delete LAS from the table in order to show 07-00 as completely reserved.

Page No: App A-119

Errata Description: The paragraph describing the EN bit is not clear.

Corrective Action: Delete the original paragraph and replace the text with: The EN bit of the VCSR_CTL register is set to a value of “1” whenever a VME64 monarch acquires the Status/ID vector for the level 2 interrupt during VME64 Auto ID.

Page No: App A-122

Errata Description: The Name VAERR[31:0] is incorrect in the VAERR Description table.

Corrective Action: Replace VAERR[31:0] with VAERR[31:1].

Page No: App A-122

Errata Description: The sentence beginning with: The Universe II PCI Master Interface, is incorrect.

Corrective Action: Replace existing text with: The Universe II VMEbus Master Interface.

Page No: App A-141

Errata Description: More information must be added to the page.

Corrective Action: Add the following sentence after the first paragraph: VCSR_BS register is accessed with an 8-bit transfer.

Page No: App A-141

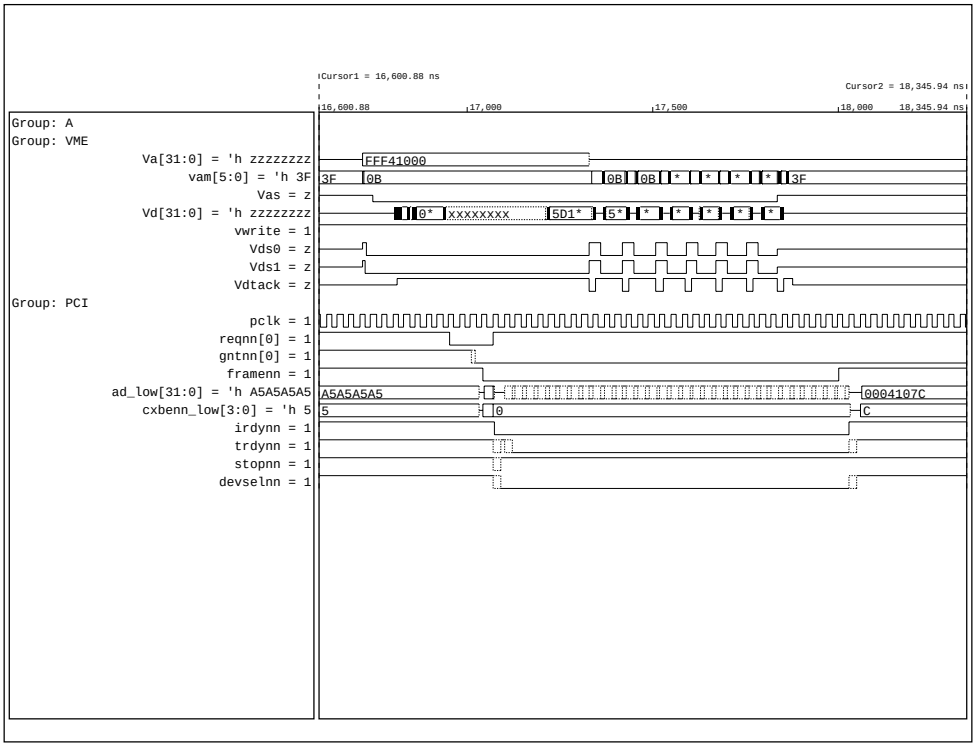
Errata Description: A note must be added to the text.

Corrective Action: The following information must be added to the text:
“Note: Bits [31:27] of the register are compared with address lines [23:19].”

Page No: App B-13

Errata Description: Figure B.11: Pre-fetched Read Cycle - Universe II as VME Slave is incorrect.

Corrective Action: Replace the existing figure with the following:



Page No: App C-3

Errata Description: Figure C.1 (continued): Universe II connections to the VMEbus Through TTL Buffers has updated table information.

Corrective Action: The table should read:

U1-U9	**‘245**
U10, U12	**‘126**
U11, U13	**‘125**
U15, U17	**‘241**

The table cell containing U14, U16 - ‘642 has been revised. This buffer type is no longer available. It is recommended that U1-U9 - ‘245 be used in its place. The input has to be tied to ground (Vss) and the enables must be used as inputs when using this buffer type. This makes the ‘245 buffer an open drain output as required.

Tundra Semiconductor Corporation
603 March Road, Kanata, Ontario Canada K2K 2M5
Tel: (613) 592-0714 or 1-800-267-7231 • Fax: (613) 592-1320

Visit our website at: www.tundra.com